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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,717	06/23/2003	Thomas Feudel	2000.106300	8735

7590 03/25/2004

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EXAMINER

LINDSAY JR, WALTER LEE

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s) AK	
	10/601,717	FEUDEL ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-48 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 21-30, 32-43 and 45-48 is/are allowed.
- 6) ☒ Claim(s) 1-20, 31 and 44 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

This Office action is in response to the application filed 6/23/03.

Currently, claims 1-48 are pending.

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the claim limitations of a semiconductive material made of silicon or germanium, must be added to the body of the specification.
2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 7, 16, 31 and 44 recite the limitation "semiconductive material" in line 1 of each claim, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior (Specification of Application No. 10/601717, pages 3-7 Figs. 1a-1d) in view of Park et al.(U.S. Patent No. 6,268,640 patented 7/31/2001).

Applicant's admitted prior art shows the method substantially as claimed, in Figs. 1a-1d and specification pages (3-7), as: forming at least one gate structure (3) above an active region of said at least one transistor (100) (Fig 1a); and implanting ions (7a) of at least one material (page 3, lines 21-23) through the portions of the surface of said substrate (1) not covered by said at least one gate structure by exposing the surface of said substrate to at least one ion beam (7a, multiple arrows) of said at least one material so as to substantially amorphize (5a)(page 3, line 23) the exposed portions of said surface to a predefined depth (Fig 1a)(page 3, lines 18-23) (claims 1 and 10).

Applicant's admitted prior art also shows, implanting ions (7h) of a first predefined conductivity type during a second implantation step (page 4, lines 2-3) through the portions of the surface of said substrate not covered by said gate structure so as to form halo structures into the amorphized portions of said substrate (Fig. 1b) (page 4, lines 2-7) (claim 10). At least one material comprises heavy inert ions, (claims 3 and 12) (page 3 lines 5-11 of the specification). The heavy inert ions comprise one of xenon, germanium, silicon, argon, or a combination (claims 4 and 13) (page 3 lines 5-11 of the specification). The implanting energy during said first implantation step is kept in the range of approximately 50-150 Kev (claims 5 and 14) (page 3 lines 5-11 of the specification). The field effect transistor is one of an NMOS and a PMOS transistor (claims 8 and 9) (Figure 1b. page 6 lines 5-9 of the specification). The method further

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comprises implanting ions of a second predefined conductivity type opposed to the first conductivity type during a third implantation step into the amorphized portions of said substrate (claim 17) (Figure 1c. page 4 lines 9-14 of the specification). The method further comprises: forming spacer elements adjacent to a portion of the sidewalls of said gate structure; and implanting ions of a predefined conductivity type corresponding to one of said first and second conductivity types during a fourth implantation step through at least the portions of said surface not covered by said gate structure and said spacer elements, (claim 18) (Figure 1d. page 4 lines 16-21 of the specification).

The admitted prior art lacks anticipation only in not expressly disclosing that: 1) at least one ion beam is kept at a tilt angle with respect to a direction perpendicular to said surface of said substrate (claims 1 and 10); 2) the tilt angle is selected between 10 and 80 degrees (claims 2 and 11); 3) the implanting dose during said first implantation step is in the range of approximately $1 \times 10^{11}/\text{cm}^2$ to $1 \times 10^{14}/\text{cm}^2$ (claims 6 and 15); 4) the substrate is rotated approximately 180 degrees about an axis perpendicular to said surface at least once during implanting (claim 9); and 5) the substrate is rotated approximately 180 degrees about an axis substantially perpendicular to said surface at least once during said first implantation step (claim 20) .

Park et al. teaches, in a similar transistor device, that non-doping ions, such as germanium, silicon, carbon or impurities such as nitrogen, at a tilt angle between 10 to about 40° , are used to amorphize the substrate (col. 3, lines 57-65). Park et al. teaches the implanting dose of $1\text{E}14 \text{ cm}^{-2}$ (col.3, lines 63-65). Park et al. also teaches rotating the substrate through 180 degrees (col. 3 line 66-col. 4 line 7).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have modified the method shown in Applicant's Admitted Prior Art, by using the tilt angle of 10 to 40 degrees, as taught in Park et al., with the motivation that Applicant's Admitted Prior Art and Park et al. are concerned with improving short channel characteristics(col. 1 lines 57-63). Additionally, the tilt angle implant of Park et al. amorphizes a region underneath the gate electrode, to allow for a reduction of lateral channeling of subsequently implanted dopants, which is an improvement over vertical implanting procedures used in Applicant's admitted prior art.

***** Note:** When applicant states that something is prior art, it is taken as being available as prior art against the claims. Admitted prior art can be used in obviousness rejections. In re Nomiya, 509 F.2d 566, 184 USPQ 607, *611 (CCPA 1975) (Figures in the application labeled "prior art" held to be an admission that what was pictured was prior art relative to applicant's invention.). ***

Allowable Subject Matter

2. Claims 21-30, 32-43, and 45-48 are allowed.

3. The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination, fails to anticipate or render obvious, the limitations of:

..."wherein the tilt angle of said ion beam with respect to a direction perpendicular to the surface of said substrate is varied according to a predefined time schedule comprising a plurality of implanting periods", as required by claims 21 and 34.

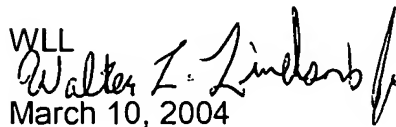
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WLL

March 10, 2004


John F. Niebling
Supervisory Patent Examiner
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